

**REMARKS****Summary of the Office Action**

Claims 1, 2, 5, and 6 stand rejected under 35 U.S.C. § 102(b) as being anticipated by *Ohzeki et al.* (U.S. Patent 4,625,241). Claims 3 and 4 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Ohzeki et al.* in view of *Sakuragi et al.* (US 2002/0109620). Claim 7 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over *Ohzeki et al.* in view of *Sakuragi et al.*, and further in view of *Yoshikawa et al.* (U.S. Patent 4,745,588).

**Summary of the Response to the Office Action**

Applicant has amended claim 1 and canceled claims 3, 4, and 7. Accordingly, claims 1, 2, 5, and 6 are pending for further consideration.

**All Claims Define Allowable Subject Matter**

Claims 1, 2, 5, and 6 stand rejected under 35 U.S.C. § 102(b) as being anticipated by *Ohzeki et al.* (U.S. Patent 4,625,241), claims 3 and 4 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Ohzeki et al.* in view of *Sakuragi et al.* (US 2002/0109620), and claim 7 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over *Ohzeki et al.* in view of *Sakuragi et al.*, and further in view of *Yoshikawa et al.* (U.S. Patent 4,745,588). Applicant respectfully traverses the rejection for at least the following reasons.

Independent claim 1, as amended, recites, in part, “a binary-coded N-bit output counter for outputting the counter clock signal by counting an input clock signal and carrying out a count operation repeatedly, said counter clock signal being selected from one of N-bit output signals in accordance with a rotation of a disk,” (emphasis added).

Page 7 of the Final Office Action admits that *Ohzeki et al.* and *Sakuragi et al.* both fail to disclose the feature “wherein said counter clock signal is selected from one of N-bit output signals in accordance with a rotation of a disk.” The Final Office Action alleges that column 6, lines 54-64 and column 7, lines 47-50 of *Yoshikawa et al.* disclose the above feature because “including a counter that counts the number pulses in accordance with optical disk rotation is advantageous because it provides a timing adjustment for the system.” Applicant respectfully disagrees.

Applicant respectfully asserts that claim 1, as amended, requires that the digitized input signal is digitized in advance by the AD converter, which includes the counter clock signal that is selected from one of N-bit output signals in accordance with a rotation of a disk. Accordingly, by using the incoming clock signal that is selected, the present invention can make the counter circuit 20 smaller compared to when a full-scale system clock signal is used.

For at least the above reasons, Applicant respectfully asserts that independent claim 1, as amended, is allowable. In addition, Applicant respectfully asserts that dependent claims 2, 5, and 6 are allowable for the same reasons set forth above.

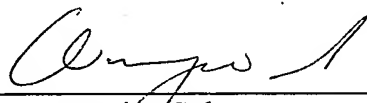
**Conclusion**

In view of the foregoing, Applicant respectfully requests reconsideration and the timely allowance of all pending claims. Should the Examiner feel that there are any issues outstanding after consideration of this response, the Examiner is invited to contact Applicant's undersigned representative to expedite prosecution.

If there are any other fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-0310.

Respectfully submitted,

**MORGAN, LEWIS & BOCKIUS LLP**

By:   
\_\_\_\_\_  
Wonjoo Suh  
Reg. No. L0296

Dated: January 23, 2008

MORGAN, LEWIS & BOCKIUS LLP  
1111 Pennsylvania Avenue, N.W.  
Washington, D.C. 20004  
(202) 739-3000